Amendments to the Claims:

Claim 1. (Currently Amended) A system ~~for generating and storing trace bits for Viterbi decoding of binary convolution codes, the system~~ comprising:

at least one arithmetic logic unit ~~(ALU) for determining~~ to determine ~~said~~ trace bits for Viterbi decoding of a binary convolution code;

a first register and a second register ~~for storing~~ to jointly store at most a single copy of said trace bits.

Claim 2. (Currently Amended) A system according to claim 1 wherein said first register ~~stores~~ is to store a first half of a series of trace bits for ~~N~~ states of said code in sequential order and said second register ~~stores~~ is to store a second half of said series in sequential order.

Claim 3. (Currently Amended) A system according to claim 2 wherein said first half comprises trace bits for a first half of said states ~~0 to N/2-1~~ and said second half comprises trace bits for a second half of said states ~~N/2 to N-1~~.

Claim 4. (Currently Amended) A system according to claim 1 and wherein said at least one ~~ALU~~ arithmetic logic unit is a first ~~ALU~~ arithmetic logic unit and a second ~~ALU~~ arithmetic logic unit and wherein said first register ~~stores~~ is to store the trace bits determined by said first ~~ALU~~ arithmetic logic unit and said second register ~~stores~~ is to store the trace bits determined by said second ~~ALU~~ arithmetic logic unit.

Claim 5. (Currently Amended) A system according to claim 1 and wherein said at least one ~~ALU~~ arithmetic logic unit is one ~~ALU~~ arithmetic logic unit ~~operating~~ to operate in split mode.

Claim 6. (Original) A system according to claim 1 and wherein said first register and said second register are shift registers.

Claim 7. (Currently Amended) A system according to claim 1, the system further comprising:

at least one barrel shifter between said first register and one of said at least one ~~ALU~~ arithmetic logic unit and between said second register and one of said at least one ~~ALU~~ arithmetic logic unit.

Claim 8. (Currently Amended) A system according to claim 2, the system further comprising:

a storage device having memory cells, wherein a group of at least one memory cell ~~stores~~ is to store said trace bits in sequential order.

Claim 9. (Currently Amended) A system according to claim 8 wherein each said group ~~stores~~ is to store the trace bits for a stage.

Claim 10. (Currently Amended) A system according to claim 8 and wherein said group ~~comprises~~ consists of one memory cell.

Claim 11. (Original) A system according to claim 10, the system further comprising:

means for packing said first half of said series of trace bits and said second half of said series of trace bits into said one memory cell so that said trace bits are packed sequentially in said memory cell.

Claim 12. (Currently Amended) A system according to claim 2, the system further comprising:

a storage device having groups of ~~P~~ memory cells, wherein the number of memory cells in each of said groups is ~~P being~~ a power of 2 and ~~P having a value of~~ is at least 2, said memory cells ~~storing~~ to store said trace bits in sequential order, wherein in each of said groups, a first half of said memory cells ~~0 to P/2-1~~ are to jointly store said first half of said series of trace bits and a second half of said memory cells ~~P/2 to P-1~~ are to jointly store said second half of said series.

Claim 13. (Currently Amended) A system according to claim ~~12 and wherein P is 2~~ 2, the system further comprising:

a storage device having groups of two memory cells to store said trace bits in sequential order, wherein in each of said groups, a first of said two memory cells is to store said first half of said series of trace bits and a second of said two memory cells is to store said second half of said series.

Claim 14. (Currently Amended) A system according to claim ~~12 and wherein P is 4~~ 2, the system further comprising:

a storage device having groups of four memory cells to store said trace bits in sequential order, wherein in each of said groups, a first two of said four memory cells are to jointly store said first half of said series of trace bits and a second two of said four memory cells are to jointly store said second half of said series.

B1 Cont.

Claim 15. (Currently Amended) A system according to claim ~~12 and wherein P is 8~~ 2, the system further comprising:

a storage device having groups of eight memory cells to store said trace bits in sequential order, wherein in each of said groups, a first four of said eight memory cells are to jointly store said first half of said series of trace bits and a second four of said eight memory cells are to jointly store said second half of said series.

Claim 16. (Currently Amended) A system according to claim ~~12 and wherein P is 16~~ 2, the system further comprising:

a storage device having groups of sixteen memory cells to store said trace bits in sequential order, wherein in each of said groups, a first eight of said sixteen memory cells are to jointly store said first half of said series of trace bits and a second eight of said sixteen memory cells are to jointly store said second half of said series.

Claim 17. (Currently Amended) A system according to claim ~~12 and wherein P is 32~~ 2, the system further comprising:

a storage device having groups of thirty-two memory cells to store said trace bits in sequential order, wherein in each of said groups, a first sixteen of said thirty-two memory cells are to jointly store said first half of said series of trace bits and a second sixteen of said thirty-two memory cells are to jointly store said second half of said series.

Claim 18. (Currently Amended) A system according to claim ~~12 and wherein P is 64~~ 2, the system further comprising:

a storage device having groups of sixty-four memory cells to store said trace bits in sequential order, wherein in each of said groups, a first thirty-two of said sixty-four memory cells are to jointly store said first half of said series of trace bits and a second thirty-two of said sixty-four memory cells are to jointly store said second half of said series.

B1 Cont.

Claim 19. (Currently Amended) A binary convolution decoder having multiple stages, each stage having ~~N~~ states of a binary convolution code, the decoder comprising:

at least one ~~ALU~~ arithmetic logic unit ~~for determining~~ to determine trace bits for each of said ~~N~~ states for each of said multiple stages;

a first register and a second register ~~for storing~~ to jointly store a single copy of trace bits of at least a portion of one stage;

a storage device having memory cells, wherein for each of said multiple stages, a group of ~~at least~~ one or more memory cells ~~cell stores~~ is to store said ~~N~~ trace bits in sequential order; and

means for tracing back, stage by stage, through said memory cells using said trace bits.

Claim 20. (Currently Amended) A decoder according to claim 19, wherein ~~each of said memory cells has a length of at least N bits and~~ said means for tracing back is ~~operative~~ to trace back in as few as two clock cycles per stage.

Claim 21. (Currently Amended) A decoder according to claim 19, wherein each of said stages has ~~N is~~ 16 states, each of said memory cells has a length of at least 16 bits and said means for tracing back is ~~operative~~ to trace back in as few as two clock cycles per stage.

Claim 22. (Currently Amended) A decoder according to claim 19, wherein each of said stages has ~~N is~~ 32 states, each of said memory cells has a length of at least 32 bits and said means for tracing back is ~~operative~~ to trace back in as few as two clock cycles per stage.

Claim 23. (Currently Amended) ~~A~~ decoder according to claim 19, the decoder further comprising:

a trace back register whose L+P-1 least significant bits indicate the location in said group of a bit whose trace bit is to be saved into the least significant bit of the trace back register after the trace back register is shifted right one bit, said location comprising the bit number given by the L least significant bits of the trace back register and the memory cell whose number in said group is given by the value in the P-1 bits of the trace back register immediately to the left of said L least significant bits, where L is the integer part of the logarithm to base 2 of the length of the memory cell and P is the number of memory cells in said group.

Claims 24 – 26 (Cancelled)

Claim 27. (Currently Amended) ~~A~~ method ~~for Viterbi decoding of binary convolution codes, the method~~ comprising ~~the steps of~~:

generating a series of trace bits for Viterbi decoding of a binary convolution code; and

storing a first half of said series sequentially in a first register and a second half of said series sequentially in a second register.

Claim 28. A method according to claim 27, wherein said first half comprises trace bits for a first half of states of said code ~~0 to N/2-1~~ and said second half comprises trace bits for a second half of said states ~~N/2 to N-1~~.

Claim 29. (Currently Amended) A method according to claim 27, the method further comprising ~~the step of~~:

saving said trace bits in sequential order to a group of ~~at least~~ one or more memory cells.

Claim 30. (Currently Amended) A method according to claim 29, wherein said group ~~comprises~~ consists of one memory cell.

Claim 31. (Currently Amended) A method according to claim 30, the method further comprising ~~the step of~~:

packing said first half of said series of trace bits and said second half of said series into said one memory cell so that said trace bits are packed sequentially in said memory cell.

Claim 32. (Currently Amended) A method according to claim 27, the method further comprising ~~the step of~~:

storing said trace bits in sequential order in groups of ~~P~~ memory cells, wherein the number of memory cells in each of said groups is ~~P being~~ a power of 2 and ~~P having a value of~~ at least 2,

wherein in each of said groups, a first half of said memory cells ~~0 to P/2-1~~ jointly store said first half of said series of trace bits and a second half of said memory cells ~~P/2 to P-1~~ jointly store said second half of said series.

Claim 33. (Currently Amended) A method according to claim ~~32 and wherein P is 2~~ 27, the method further comprising:

storing said trace bits in sequential order in groups of two memory cells, wherein in each of said groups, storing said trace bits comprises storing said first half of said series of trace bits in a first of said two memory cells and storing said second half of said series of trace bits in a second of said two memory cells.

Claim 34. (Currently Amended) A method according to claim ~~32 and wherein P is 4~~ 27, the method further comprising:

storing said trace bits in sequential order in groups of four memory cells, wherein in each of said groups, storing said trace bits comprises storing said first half of said series of trace bits in a first two of said four memory cells and storing said second half of said series of trace bits in a second two of said four memory cells.

Claim 35. (Currently Amended) A method according to claim ~~32 and wherein P is 8~~ 27, the method further comprising:

storing said trace bits in sequential order in groups of eight memory cells, wherein in each of said groups, storing said trace bits comprises storing said first half of said series of trace bits in a first four of said eight memory cells and storing said second half of said series of trace bits in a second four of said eight memory cells.

Claim 36. (Currently Amended) A method according to claim ~~32 and wherein P is 16~~ 27, the method further comprising:

storing said trace bits in sequential order in groups of sixteen memory cells, wherein in each of said groups, storing said trace bits comprises storing said first half of said series of trace bits in a first eight of said sixteen memory cells and storing said second half of said series of trace bits in a second eight of said sixteen memory cells.

Claim 37. (Currently Amended) A method according to claim ~~32 and wherein P is 32~~ 27, the method further comprising:

storing said trace bits in sequential order in groups of thirty-two memory cells, wherein in each of said groups, storing said trace bits comprises storing said first half of said series of trace bits in a first sixteen of said thirty-two memory cells and storing said second half of said series of trace bits in a second sixteen of said thirty-two memory cells.

Claim 38. (Currently Amended) A method according to claim ~~32 and wherein P is 64~~ 27, the method further comprising:

storing said trace bits in sequential order in groups of sixty-four memory cells, wherein in each of said groups, storing said trace bits comprises storing said first half of said series of trace bits in a first thirty-two of said sixty-four memory cells and storing said second half of said series of trace bits in a second thirty-two of said sixty-four memory cells.

Claim 39. (Currently Amended) ~~A~~ method for Viterbi decoding of binary convolution codes, the decoding involving multiple stages each having ~~N~~ states of a binary convolution code, the method comprising ~~the steps of~~:

determining trace bits ~~for each storing said trace bits~~ for each of said ~~N~~ states for each of said multiple stages;

storing a single copy of trace bits of at least a portion of one stage jointly in a ~~girst~~ first register and a second register;

for each of said multiple stages, storing said ~~N~~ trace bits in sequential order in a group of ~~at least~~ one or more memory cells ~~cell~~; and

tracing back, stage by stage, through said memory cells using said trace bits.

B' Cont.

Claim 40. (Currently Amended) A method according to claim 39, wherein ~~each of said memory cells has a length of at least N bits and said step of~~ tracing back through said memory cells is performed in as few as two clock cycles per stage.

Claim 41. (Currently Amended) A method according to claim 39, wherein each of said stages has ~~N is~~ 16 states, each of said memory cells has a length of at least 16 bits and ~~said step of~~ tracing back through said memory cells is performed in as few as two clock cycles per stage.

Claim 42. (Currently Amended) A method according to claim 39, wherein each of said stages has ~~N is~~ 32 states, each of said memory cells has a length of at least 32 bits and ~~said step of~~ tracing back through said memory cells is performed in as few as two clock cycles per stage.

Claim 43. (Currently Amended) A method according to claim 39, wherein ~~said step of~~ tracing back through said memory cells comprises for each stage ~~the step of~~:

shifting a trace back register right one bit;

saving into the least significant bit of said trace back register the trace bit located in the memory cell whose number in said group is given by the value of the P-1 bits of said trace back register immediately to the left of the L least significant bits of said trace back register and located at the bit number given by said L least significant bits of said trace back register, where L is the integer part of the logarithm to base 2 of the length of the memory cell and P is the number of memory cells in said group.